

WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:
 - a substrate including a plurality of pixel areas;
 - a semiconductor layer formed on the substrate and including a plurality of pairs of first and second semiconductor portions in respective pixel areas;
 - a first insulating layer formed on the semiconductor layer;
 - a gate wire formed on the first insulating layer;
 - a second insulating layer formed on the gate wire;
 - a data wire formed on the second insulating layer;
 - 10 a third insulating layer formed on the data wire;
 - a pixel electrode formed on the third insulating layer and connected to the data wire,
 - wherein width and length of at least one of the first and the second semiconductor portions vary between at least two pixel areas.
- 15 2. The thin film transistor array panel of claim 1, further comprising:
 - a plurality of partitions for defining the pixel areas; and
 - a plurality of organic light emission members formed on the pixel electrodes.
- 20 3. The thin film transistor array panel of claim 1, wherein the semiconductor layer further includes a plurality of storage electrode portions,
 - the gate wire includes a plurality of first and second gate electrodes and storage electrodes overlapping the first and the second semiconductor portions and the storage electrode portions, respectively,
 - 25 each of the first and the second semiconductor portions has a channel region, a source region, and a drain region, and
 - the data wire includes a plurality of first and second data lines, a plurality of first source electrodes connected to the first data lines and to the source regions of the first semiconductor portions, a plurality of first drain electrodes connected to the drain regions of the first semiconductor portions and to the second gate electrodes, a plurality of second source electrodes connected to the second data lines and to the source regions of the second semiconductor
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portions, and a plurality of second drain electrodes connected to the drain regions of the second semiconductor portions and to the pixel electrodes.

4. A thin film transistor array panel comprising:
 - a plurality of first thin film transistors;
 - 5 a plurality of second thin film transistors connected to the first thin film thin film transistors and including channel regions having at least two widths and lengths; and
 - a plurality of pixel electrodes connected to the second thin film transistors.
- 10 5. The thin film transistor array panel of claim 4, wherein the channel regions comprise polysilicon.
- 15 6. The thin film transistor array panel of claim 4, wherein each of the first and the second thin film transistors has a gate, a source, and a drain, and the gates of the second thin film transistors are connected to the drains of the first thin film transistors.